AMENDMENTS TO THE CLAIMS

Please cancel Claims 1-15; amend Claims 16-19; and add new Claims 20-45 as follows. The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1-15. (cancelled)

16. (currently amended) A method of manufacturing a semiconductor, comprising steps of:

~~basic structure forming step for~~ forming a basic structure of a semiconductor device on a semiconductor wafer;

~~passivation film forming step for~~ forming a final passivation film that transmits ultra violet rays on an uppermost of the basic structure;

~~bias voltage applying step for~~ applying a bias voltage to the semiconductor device, the ~~with a~~ bias voltage having a predetermined level voltage that can maintain the semiconductor device with turning of f; and

~~ultra violet rays radiation step conducted after the bias voltage applying step, for~~ radiating ultra violet rays to the basic structure of the semiconductor device through the final passivation film after the step of applying the bias voltage.

17. (currently amended) A method of manufacturing a semiconductor device, comprising steps of:

~~basic structure forming step for~~ forming a basic structure of a semiconductor device on a semiconductor wafer;

~~passivation film forming step for~~ forming a final passivation film that transmits ultra violet rays on an uppermost of the basic structure;

~~division step for~~ dividing the semiconductor device into a plurality of semiconductor chips;

~~packaging step for~~ mounting the semiconductor chip on a package having a transmitting portion that can transmit ultra violet rays at least on the final passivation film side;

~~bias voltage applying step for~~ applying a bias voltage to the semiconductor device, the ~~with a~~ bias voltage having a predetermined level voltage that can maintain the semiconductor device with turning off; and

~~ultra violet rays radiation step conducted after the bias voltage applying step, for~~ radiating ultra violet rays to the basic structure of the semiconductor device through the transmitting portion and the final passivation film after the step of applying the bias voltage.

18. (currently amended) A method of manufacturing a semiconductor according to ~~claim~~ Claim 16, wherein:

the semiconductor is a switching element selected from one of a LDMOS FET (Lateral Double-Diffused Metal Oxide Semiconductor Field effect Transistor) and a VDMOS FET (Vertical Double-Diffused Metal Oxide Semiconductor Field effect Transistor)[[,]] ; and

the bias voltage applying step applies the bias voltage between a source and a drain of the switching element ~~with the bias voltage having a predetermined level voltage that can maintain the switching element with turning off~~.

19. A method of manufacturing a semiconductor according to ~~claim~~ Claim 16, wherein the ultra violet rays radiation step radiates ultra violet rays having a band whose wave length of 253.7 nm.

20. (new) A method of manufacturing a semiconductor according to Claim 17, wherein:

the semiconductor is a switching element selected from one of a LDMOS FET (Lateral Double-Diffused Metal Oxide Semiconductor Field effect Transistor) and a VDMOS FET (Vertical Double-Diffused Metal Oxide Semiconductor Field effect Transistor); and

the bias voltage applying step applies the bias voltage between a source and a drain of the switching element.

21. (new) A method of manufacturing a semiconductor according to Claim 17, wherein the ultra violet rays radiation step radiates ultra violet rays having a band whose wave length of 253.7 nm.

22. (new) A method of manufacturing a semiconductor device according to Claim 16, wherein the step of forming the basic structure includes:

forming a transistor structure, formed in a semiconductor substrate defined in said semiconductor wafer, comprising a drain region, a source region formed in a channel well layer and a gate electrode, formed on the semiconductor substrate, with a gate oxide film interposed between said gate electrode and a channel forming region formed in said channel well layer, said transistor structure further comprising an insulating isolation film formed between said drain region and said channel well layer, wherein:

the gate electrode is formed so as to extend toward the drain region to have a portion overlapping with the insulating isolation film, and said gate electrode is formed so that a maximum electric field point in the neighborhood of a surface of the semiconductor substrate occurs at substantially the center portion of a region corresponding to the insulating isolation film, when a predetermined bias voltage is applied between the source region and the drain region, and the source region and the gate electrode are at substantially identical potential.

23. (new) A method of manufacturing a semiconductor device according to Claim 16, wherein the step of forming the basic structure includes:

forming a transistor structure, formed in a semiconductor substrate defined in said semiconductor wafer, comprising a drain region, a source region formed in a channel well layer and a gate electrode, formed on the semiconductor substrate, with a gate oxide film interposed between said gate electrode and a channel forming region formed in said channel well layer, said transistor structure further comprising an

insulating isolation film formed between said drain region and said channel well layer, wherein:

the gate electrode extends toward the drain region so as to have a portion overlapping with the insulating isolation film, and said gate electrode is formed so that a peak carrier generation rate in the neighborhood of a surface of the semiconductor substrate occurs at lower region corresponding to the insulating isolation film, when a predetermined bias voltage is applied between the source region and the drain region, and the source region and the gate electrode are at substantially identical potential.

24. (new) A method of manufacturing a semiconductor device according to Claim 16, wherein the step of forming the basic structure includes:

forming a transistor structure, formed in a semiconductor substrate defined in said semiconductor wafer, comprising a drain region, a source region formed in a channel well layer and a gate electrode, formed on the semiconductor substrate, with a gate oxide film interposed between said gate electrode and a channel forming region formed in said channel well layer, said transistor structure further comprising an insulating isolation film formed between said drain region and said channel well layer, wherein:

the gate electrode extends toward the drain region so as to have a portion overlapping with the insulating isolation film, and said gate electrode is formed so that a carrier flow in the neighborhood of a surface of the semiconductor substrate contains a component toward an opposite side direction of the insulating isolation film, when a

predetermined bias voltage is applied between the source region and the drain region, and the source region and the gate electrode are at substantially identical potential.

25. (new) A method of manufacturing a semiconductor device according to Claim 22, wherein said gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to or more than substantially a half of a width size of the insulating isolation film.

26. (new). A method of manufacturing a semiconductor device according to Claim 23, wherein said gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to or more than substantially a half of a width size of the insulating isolation film.

27. (new) A method of manufacturing a semiconductor device according to Claim 24, wherein said gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to or more than substantially a half of a width size of the insulating isolation film.

28. (new) A method of manufacturing a semiconductor device according to Claim 25, wherein said gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to substantially a half of a width size of the insulating isolation film.

29. (new) A method of manufacturing a semiconductor device according to Claim 26, wherein said gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to substantially a half of a width size of the insulating isolation film.

30. (new) A method of manufacturing a semiconductor device according to Claim 27, wherein said gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to substantially a half of a width size of the insulating isolation film.

31. (new) A method of manufacturing a semiconductor device according to Claim 22, wherein the step of forming the basic structure includes:

preparing an SOI substrate wafer formed from a supporting substrate and a semiconductor layer with an insulating film interposed therebetween, wherein said transistor structure is formed in said semiconductor layer.

32. (new) A method of manufacturing a semiconductor device according to Claim 31, wherein the supporting substrate is made of semiconductor material, and the supporting substrate includes a potential fixing electrode formed on its back surface to fix a potential of the supporting substrate with a predetermined level.

33. (new) A method of manufacturing a semiconductor device according to Claim 16, wherein the step of forming the basic structure includes:

forming a transistor structure, formed in a semiconductor substrate defined in said semiconductor wafer, comprising a drain region having a P-type conductivity, a source region, formed in a channel well layer of a N-type conductivity, having a P-type conductivity, and a gate electrode, formed on the semiconductor substrate, with a gate oxide film interposed between said gate electrode and a channel forming region formed in said channel well layer, said transistor structure further comprising an insulating isolation film formed between said drain region and said channel well layer, wherein:

the gate electrode is disposed at a side of said insulating isolation film opposite to a location where the drain region is formed, the gate electrode extends toward the drain region so as to have a portion overlapping with the insulating isolation film, and said gate electrode is formed so that a maximum electric field point in the neighborhood of a surface of the semiconductor substrate occurs at substantially the center portion of a region corresponding to the insulating isolation film, when a predetermined bias voltage is applied between the source region and the drain region, and the source region and the gate electrode are at substantially identical potential.

34. (new) A method of manufacturing a semiconductor device according to Claim 17, wherein the step of forming the basic structure includes:

forming a transistor structure, formed in a semiconductor substrate defined in said semiconductor wafer, comprising a drain region, a source region formed in a channel well layer and a gate electrode, formed on the semiconductor substrate, with a gate oxide film interposed between said gate electrode and a channel forming

region formed in said channel well layer, said transistor structure further comprising an insulating isolation film formed between said drain region and said channel well layer, wherein:

the gate electrode is formed so as to extend toward the drain region to have a portion overlapping with the insulating isolation film, and said gate electrode is formed so that a maximum electric field point in the neighborhood of a surface of the semiconductor substrate occurs at substantially the center portion of a region corresponding to the insulating isolation film, when a predetermined bias voltage is applied between the source region and the drain region, and the source region and the gate electrode are at substantially identical potential.

35. (new) A method of manufacturing a semiconductor device according to Claim 17, wherein the step of forming the basic structure includes:

forming a transistor structure, formed in a semiconductor substrate defined in said semiconductor wafer, comprising a drain region, a source region formed in a channel well layer and a gate electrode, formed on the semiconductor substrate, with a gate oxide film interposed between said gate electrode and a channel forming region formed in said channel well layer, said transistor structure further comprising an insulating isolation film formed between said drain region and said channel well layer, wherein:

the gate electrode extends toward the drain region so as to have a portion overlapping with the insulating isolation film, and said gate electrode is formed so that a peak carrier generation rate in the neighborhood of a surface of the semiconductor

substrate occurs at lower region corresponding to the insulating isolation film, when a predetermined bias voltage is applied between the source region and the drain region, and the source region and the gate electrode are at substantially identical potential.

36. (new) A method of manufacturing a semiconductor device according to Claim 17, wherein the step of forming the basic structure includes:

forming a transistor structure, formed in a semiconductor substrate defined in said semiconductor wafer, comprising a drain region, a source region formed in a channel well layer and a gate electrode, formed on the semiconductor substrate, with a gate oxide film interposed between said gate electrode and a channel forming region formed in said channel well layer, said transistor structure further comprising an insulating isolation film formed between said drain region and said channel well layer, wherein:

the gate electrode extends toward the drain region so as to have a portion overlapping with the insulating isolation film, and said gate electrode is formed so that a carrier flow in the neighborhood of a surface of the semiconductor substrate contains a component toward an opposite side direction of the insulating isolation film, when a predetermined bias voltage is applied between the source region and the drain region, and the source region and the gate electrode are at substantially identical potential.

37. (new) A method of manufacturing a semiconductor device according to Claim 34, wherein said gate electrode is formed so that a protrusion amount onto the

insulating isolation film is set equal to or more than substantially a half of a width size of the insulating isolation film.

38. (new). A method of manufacturing a semiconductor device according to Claim 35, wherein said gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to or more than substantially a half of a width size of the insulating isolation film.

39. (new) A method of manufacturing a semiconductor device according to Claim 36, wherein said gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to or more than substantially a half of a width size of the insulating isolation film.

40. (new) A method of manufacturing a semiconductor device according to Claim 37, wherein said gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to substantially a half of a width size of the insulating isolation film.

41. (new) A method of manufacturing a semiconductor device according to Claim 38, wherein said gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to substantially a half of a width size of the insulating isolation film.

42 (new) A method of manufacturing a semiconductor device according to Claim 39, wherein said gate electrode is formed so that a protrusion amount onto the insulating isolation film is set equal to substantially a half of a width size of the insulating isolation film.

43. (new) A method of manufacturing a semiconductor device according to Claim 34, wherein the step of forming the basic structure includes:

preparing an SOI substrate wafer formed from a supporting substrate and a semiconductor layer with an insulating film interposed therebetween, wherein said transistor structure is formed in said semiconductor layer.

44. (new) A method of manufacturing a semiconductor device according to Claim 43, wherein the supporting substrate is made of semiconductor material, and the supporting substrate includes a potential fixing electrode formed on its back surface to fix a potential of the supporting substrate with a predetermined level.

45. (new) A method of manufacturing a semiconductor device according to Claim 17, wherein the step of forming the basic structure includes:

forming a transistor structure, formed in a semiconductor substrate defined in said semiconductor wafer, comprising a drain region having a P-type conductivity, a source region, formed in a channel well layer of a N-type conductivity, having a P-type conductivity, and a gate electrode, formed on the semiconductor substrate, with a gate oxide film interposed between said gate electrode and a channel

forming region formed in said channel well layer, said transistor structure further comprising an insulating isolation film formed between said drain region and said channel well layer, wherein:

the gate electrode is disposed at a side of said insulating isolation film opposite to a location where the drain region is formed, the gate electrode extends toward the drain region so as to have a portion overlapping with the insulating isolation film, and said gate electrode is formed so that a maximum electric field point in the neighborhood of a surface of the semiconductor substrate occurs at substantially the center portion of a region corresponding to the insulating isolation film, when a predetermined bias voltage is applied between the source region and the drain region, and the source region and the gate electrode are at substantially identical potential.